Elizabeth Mountz

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SUMMARY

ECE Masters student at Carnegie Mellon University graduating in December 2024 with a specialty in analog/mixed-signal integrated circuit design and photonic MEMS design. Seeking full-time opportunities to expand design portfolio in integrated sensing/wireless communications applications.

EDUCATION

CARNEGIE MELLON UNIVERSITY   Pittsburgh, PA
Master of Electrical Engineering   12/24
GPA: 3.92
- **THESIS:** Acousto-Optic Resonator Design for Beam Steering Applications
- **RELEVANT GRADUATE COURSEWORK:** Analog IC Design; Advanced Digital IC Design; RF IC Implementation; IC Verification; Design, Integration, and Tape-out of IoT Systems; Nanofabrication Lab; Computational Photography
- **AFFILIATIONS:** Micro and Nano Systems Laboratory, Integrated Circuits and Bioengineering Lab, Biorobotics Lab
- **INTERESTS:** Private Pilot License, Carnegie Mellon University Small Ensemble (Oboist)

UNIVERSITY OF PITTSBURGH   Pittsburgh, PA
Bachelor of Science in Bioengineering   5/22
GPA: 3.6

EXPERIENCE

QORVO   Fort Lauderdale, FL
Analog IC Design Intern   5/24-8/24
- Completed comprehensive training in SPICE simulation tools
- Presented circuit design and simulation results to broader SoC engineering and executive team
- Ported switched capacitor scaler circuit to advanced technology node and characterized analog switch design charge injection, speed, static/dynamic power consumption, and DC impedance

MIXED-SIGNAL TAPEOUT; DIRECT DIGITAL SYNTHESIZER   Pittsburgh, PA
Course Project; CMU-Apple Silicon Initiative   1/24-5/24
- Proposed mixed-signal Direct Digital Synthesis (DDS) chip for ultrasonic transducer phased array control
- Designed in Cadence Virtuoso with 22nm TSMC Process 8-bit unary current steering DAC schematic and layout
- Characterized in simulation DAC performance at temperature/power/process corners

MIXED-SIGNAL TAPEOUT; CMOS IMAGE SENSOR   Pittsburgh, PA
Course Project; CMU-Apple Silicon Initiative   8/24-present
- Learning fundamentals of system-level chip design, including digital timing, peripheral circuitry, and whole chip integration/simulation
- Working in teams on circuit design blocks in Cadence (65nm TSMC process), including DAC, comparator, counter, scan chain, I/O, digital processor

CHIP VERIFICATION   Pittsburgh, PA
Course Project; CMU-Apple Silicon Initiative   8/24-present
- Verifying previous direct digital synthesizer chip tape-out by designing and fabricating a test PCB, conducting chip bring-up, and debugging any unexpected behaviors

MICROELECTROMECHANICAL SYSTEMS (MEMS) DESIGN   Pittsburgh, PA
Graduate Research   8/23 – present
- Optimized electro-mechanical coupling coefficient in Surface Acoustic Wave (SAW) transducer design using COMSOL Multiphysics simulation with ongoing objective of fabricating the device with the optimized parameters
- Configured and documented cloud computing and batch processing methods for faster parameter sweeps in transducer simulations

HEBI ROBOTICS   Pittsburgh, PA
Electrical Engineering Intern   5/23 – 8/23
- Designed schematic and PCB layout in Altium for internal development use including 4-channel Ethernet/optical fiber switch, 4-channel brushed DC motor driver with motor coil current sensing, and a 160W Eload with active cooling, on-board current/voltage sensing, and thermal regulation.

SKYDIO   San Francisco, CA
Electrical Engineering Intern   5/22 – 12/22
- Designed schematic and 6-layer PCB in Cadence PCB Suite for two iterations of a product, and a test fixture board
- Collaborated with product development team to meet size constraints of product form-factor and with the system integration team for final component testing and selection
- Worked closely with firmware team on STM32 MCU selection, integration in design, and firmware bring-up

SKILLS

- Analog/Mixed-Signal/RF IC Design
- SPICE Simulation
- Cadence Virtuoso ADE and Layout Suite
- COMSOL Multiphysics Simulation
- Nanofabrication
- Multi-Layer PCB Design (Cadence and Altium)
- Optical System Design and Simulation (Ansys)
- Image Processing